SF389 PIR Circuit IC

PASSIVE INFRA-RED ALARM

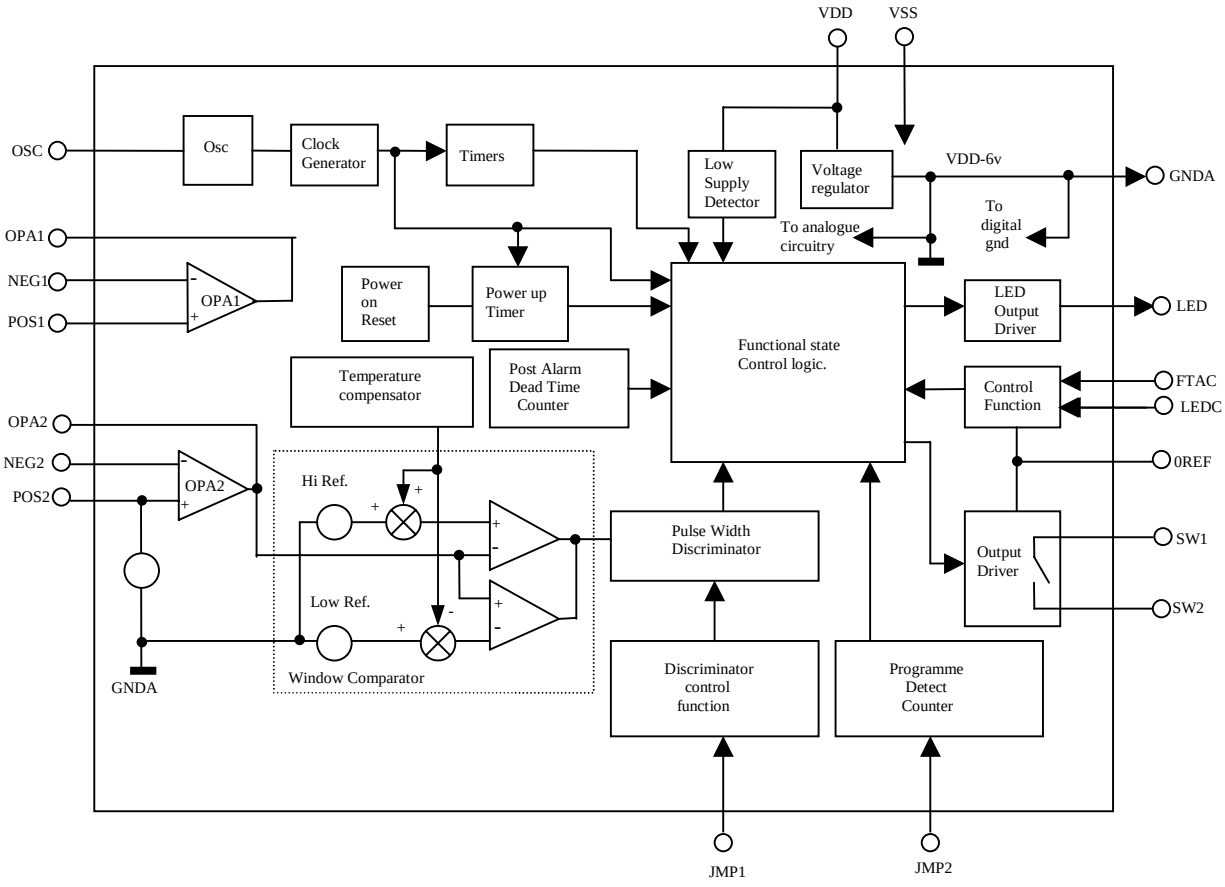
Preliminary datasheet

The SF389 is a CMOS, mixed signal ASIC designed for PIR motion detection and similar alarm applications. The ASIC interfaces directly between a Pyroelectric Infrared (PIR) sensor and control panel using a normally closed, low impedance solid state switch. Alternatively the output can drive a conventional low power relay. The product includes several additional functions not normally included in discrete circuit based designs, which enhance its performance and capabilities at both the individual sensor unit and control panel levels during product manufacture and end installation.

FEATURES.

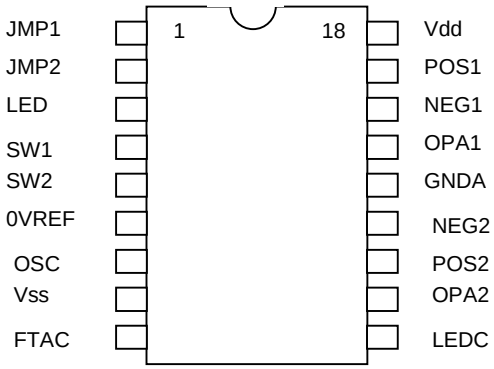
- Flexible input stage.
- Precision on-chip reference and threshold comparators.
- Pin programmable pulse count and pulse width discrimination.
- Temperature compensated sensitivity.
- Alarm event capture.
- Remote control of status LED.
- Local status diagnostic display.

1.0 BLOCK DIAGRAM



2.0 PIN CONFIGURATION

These devices have been designed to withstand up to 1kV of electrostatic discharge between pin pairs. As such, precautions must be taken to ensure that the device is not damaged during handling and transportation.



2.1 PIN DESCRIPTION for 18 PDIP

NAME	PIN	TYPE	FUNCTION
JMP1	1	Digital Input, 3 state.	Selection of 3 debounce period choices. Input may be returned to Vdd, Vss or remain floating.
JMP2	2	Digital Input, 3 state.	Selection of 3 pulse count choices. Input may be returned to Vdd, Vss or remain floating.
LED	3	Digital Output	Driver for LED. Connect through resistor and LED to VSS.
SW1	4	Digital Output	One pole of the internal, bi-directional analogue switch, which is the main output of the ASIC.
SW2	5	Digital Output	Second pole of the internal, bi-directional analogue switch.
OVREF	6	Supply	Provides internal bias for interfacing circuitry included in FTAC, LEDC and SW1 & SW2. Normally connected to Vss via a resistor.
OSC	7	Analogue Input	Oscillator timing resistor and capacitor. Both are connected in parallel from OSC to Vdd.
VSS	8	Supply	Negative supply
FTAC	9	Digital Input	First To Alarm Control input. May be left open circuit because it has an on chip resistor to Vss.
LEDC	10	Digital Input	LED Control input. May be left open circuit because it has an on chip resistor to Vss.
OPA2	11	Analogue Output	Output of input amplifier 2
POS2	12	Analogue Input	Internal bias point for the non-inverting input of amplifier 2
NEG2	13	Analogue Input	Inverting input of amplifier 2
GNDA	14	Analogue Output	Output of the internal voltage regulator. Nominal value is -6 volts with respect to Vdd
OPA1	15	Analogue Output	Output of input amplifier 1
NEG1	16	Analogue Input	Inverting input of amplifier 1
POS1	17	Analogue Input	Non-inverting input of amplifier 1
VDD	18	Supply	Positive supply

3.0 ABSOLUTE MAXIMUM RATINGS

Rating	**Value**	**Unit**
DC supply voltage Vdd -Vss	-0.5 to +16	Vdc
Input voltage for JMPI, JMP2 FTAC, LEDC inputs	Vss-O 5 to Vdd+O 5	Vdc
Input voltage for Osc, POSI NEGI, POS2, NEG2	GNDA-0.5 to Vdd+0.5	Vdc
Max power dissipation per output	100	mW
Total dissipation of packaged device	200	mW
Storage Temperature Range	-65 to +150	°C
Max current into or out of any pin	30	mA

4.0 ELECTRICAL SPECIFICATION

Parameter	Min	Typ	Max	Unit
Operating voltage	7.0	12	16	V
Operating temperature range	-25		55	°C
Oscillator frequency using 470KΩ 1% and 1000pF, NPO capacitor	2.0	2.1	2.2	kHz
Off impedance of SW1 to SW2	?			Ω
Current sourced or sunk from SW1/SW2.			20	mA
On resistance Between SW1 and SW2.		45	60	Ω
Off voltage at LED output	0		Vdd	Vdc
Current sourced from LED output			20	mA
Voltage at LED output while sinking 10mA	Vdd-0.8		Vdd	Vdc
Under voltage cut-in threshold (Vdd -Vss)	7.7	8.0	8.3	Vdc
Under voltage cut-out threshold(Vdd-Vss)	Cut in +0.2V			

Regulator Characteristics

Parameter	Min	Typ	Max	Units
Supply voltage (Vdd-Vss)	7.5	12.0	16.0	Vdc
Regulated output voltage wrt Vdd	-5.7	-6.0	-6.3	Vdc
Regulator output current between Vdd and GNDA	0.2		5.0	mA
Quiescent current			0.2	mA
Line regulation			50	mV
Load regulation		50		mV
Ripple rejection at 120Hz			50.0	mV

Op Amp 1 Characteristics (Voltages wrt GNDA)

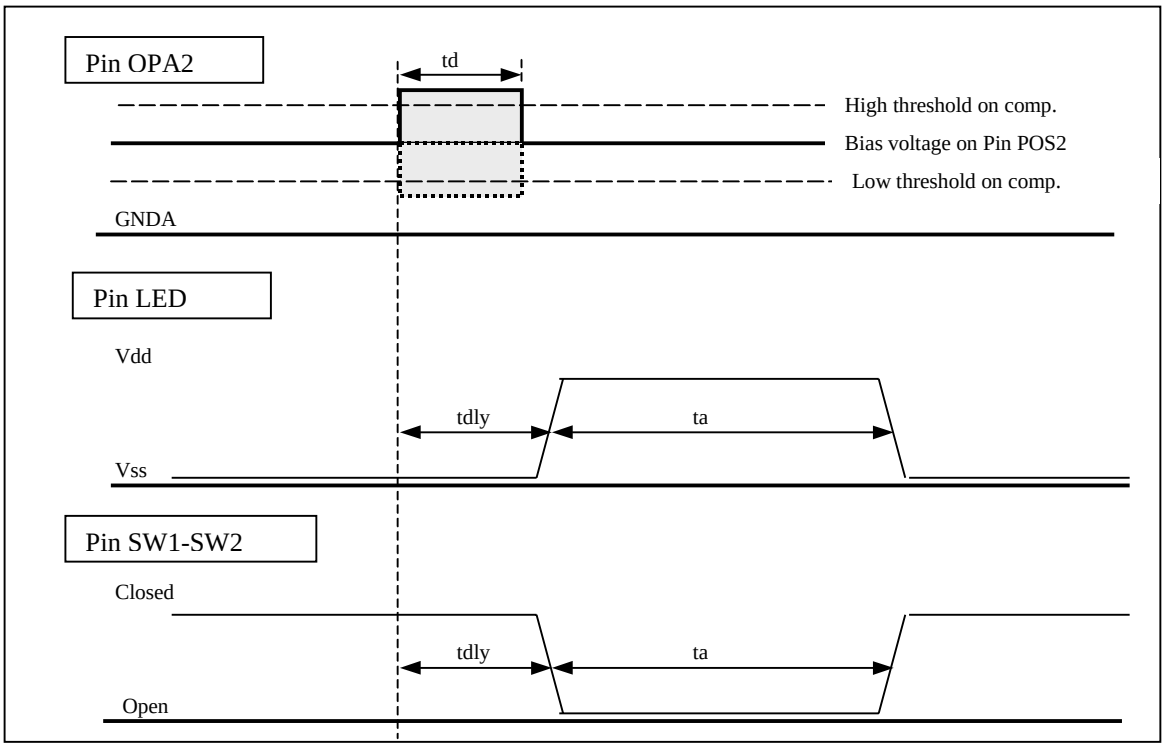
Parameter	Min	Typ	Max	Unit
Large signal voltage amplification	4.0			V/mV
Input offset voltage		5.0	20.0	mV
Input common mode range	0.2	to	Vdd-2	V
Output voltage range (unloaded)	0	to	Vdd-2	V
Quiescent current			100	µA
Common mode rejection ratio	65			dB
Supply voltage rejection ratio	65			dB
Input noise current (1kHz BW)			50	fA/Hz
Input noise voltage (1kHz BW)			50	nV/Hz

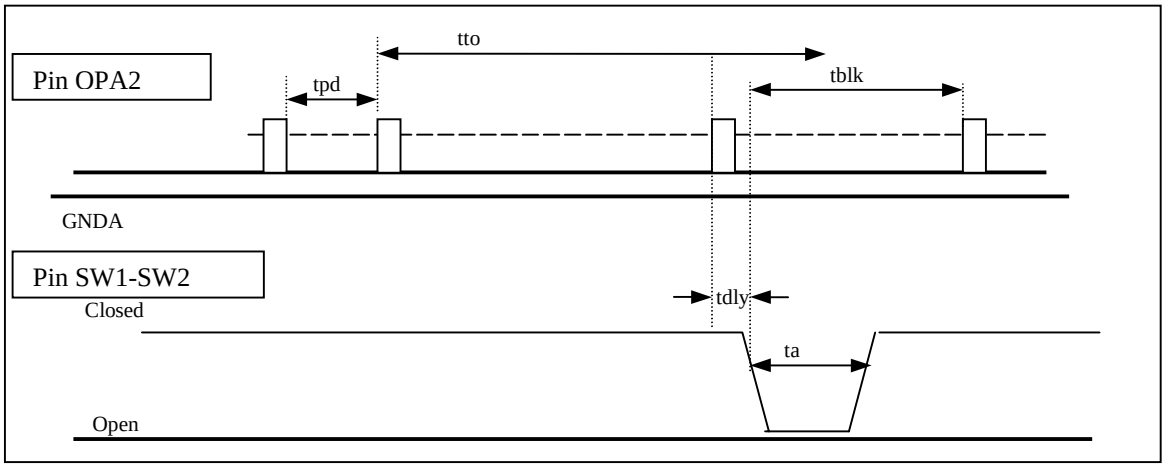
Op-amp 2 characteristics (voltages wrt GNDA)

Parameter	Min	Typ	Max	Unit
Large signal voltage amplification	4.0			V/mV
Input offset voltage		5.0	20	mV
Input common mode range	2.0	to	Vdd-1	V
Output voltage range (unloaded)	0.5	to	Vdd-0.5	V
Quiescent current			100	µA
Common mode rejection ratio	65			dB
Supply voltage rejection ratio	65			dB
Input noise current (1kHz BW)			5-	fA/Hz
Input noise voltage (1KHz BW)			50	nV/Hz

Note: When op-amp2 is used as an inverting amplifier, the DC offset will be multiplied by the DC gain which would move the output operating point away from the mid point between the upper and lower trip points of the window comparator. This would cause an asymmetric system gain response between positive and negative signals from the PIR detector. To counteract this, the ASIC is trimmed during manufacture to centre the output of op-amp2 at the mid-pint between the window comparator trip points.

4.1 TIMING or TEST DEFINITION DIAGRAM





Timing for JMP2 =Vdd,
Conditions for JMP2=open are similar

5.0 GENERAL DESCRIPTION

The SF389 PIR alarm IC is targeted at panel based intruder alarm systems. The architecture allows a wide range of functions to be selected and optimised at the unit design level and the post installation stage.
Operation of the functional blocks shown in the block diagram are discussed in detail below.

6.0 DESCRIPTION OF FUNCTION

Input Amplification.

The input operational amplifiers OPA1 and OPA2 are normally used to amplify and filter the low level sensor signal to signal amplitudes greater than the window comparator threshold. They are typically used together configured as a bandpass filter employing external components to program the required pass-band gain and bandwidth performance. A typical design example is included in later section of this specification.

Front End Amplifier.

OPA1, is an uncommitted op-amp with a common mode input voltage range optimised for low side referenced signals. This makes it possible to DC couple directly to industry standard PIR detector elements such as the Heimann LHi 958, or LHi 954.
The normal configuration is as a non-inverting stage with external components selected to provide the main pole and zero bandpass filter.

Second Stage Amplifier.

OP AMP2, provides more pass band gain and provides another pole and zero for the bandpass filter. The basic function is to boost the signal from the first stage amplifier to the level required to drive the Window Comparator section.
AC coupling is used between stages to improve the low frequency roll off the filter and a DC offset is introduced internally on pin POS2 to bias the level on pin OPA2 midway between the window comparator HI and LO thresholds.
Together the two amplifiers would normally be configured to implement a two stage band pass filter with a nominal voltage gain of around 3100 (70dB) at signal input frequency f= 1Hz often used in PIR applications.

Oscillator Clock Generator and Timer

The internal clock generator and dividers provide the main timebase for the ASIC and therefore the various timing signals. The timer delays specified are directly related to the internal timing signals and therefore oscillator accuracy. One useful effect of this is that test time during product manufacture can be reduced by increasing the clock frequency by a factor of 2 or 4 times.

The frequency of the oscillator is set by an external resistor, R, and capacitor, C. The oscillator period, Tf, is calculated simply using $Tf=RC + 5\ \mu s$, where the units of R is ohms and C is farads.. With $R = 470k\Omega$ and C = 1000pF, the oscillator frequency (1/Tf) will be close to 2100Hz.

The ratiometric design ensures that the frequency is largely independent of the supply voltage over the specified range. The characteristics of R and C therefore dominate the accuracy and temperature stability of the timing.

Window Comparator

The performance of the comparator block, and subsequent processing of its output signal internally, is the key to providing accurate and reliable event detection. The relationship between the switching points of the comparator and its bias point in conjunction with the gain of the input section, determines the sensitivity of the detection system.
The circuitry is arranged so that at 25.deg. C, the comparator threshold is set to nominally 1 volt above and below a DC bias voltage connected to pin POS2. This condition is set during ASIC manufacture to minimise errors.

Voltage Regulator

The ASIC has an internal nominal 6V regulator, which it uses to provide the internal power supply for the analogue and digital circuit blocks. The output of the regulator is available externally to provide a regulated power supply for the sensor element and other circuitry where required.
The regulator is referenced to the positive side of the power input to the module (VDD). This is a consequence of the P-well CMOS technology which is used to manufacture this ASIC. Signals from the control panel to the module will normally be referenced to the panel negative supply, but the ASIC has internal level shifting circuits at the control inputs to allow them to interface with the internal logic circuits.

Internal Temperature Adjustment of Detection Sensitivity

It is a common requirement of PIR motion detection alarms that the sensitivity can be adjusted with temperature. This is to compensate for the fact that the PIR element is responding to the difference between the temperature of the target and the background ambient.
The SF389 has an on chip ambient temperature detector which is used to adjust the system sensitivity by varying the height of the window comparator above the op-amp 2 trip points. For colder ambients the sensitivity is reduced, and for hotter ambients the sensitivity is increased above the norm at 25C.

This feature is useful only in installations where the ambient temperature in the module location is always approximately the same as the ambient temperature of the detection zone. It is important to ensure that the module does not have any significant internal self-heating mechanism, which might cause an unexpected increase in sensitivity.

If required, versions of the ASIC could be supplied with the temperature adjustment action disabled.

Externally Programmable Detect Pulse Discrimination.

As an aid to prevention of false alarms, the SF389 contains two powerful discrimination blocks which examine the output from the window comparator to determine if the detect pulse is a valid alarm.

These blocks are completely digital. The first of them is the de-bounce or pulse width discriminator circuit. The condition is that the amplitude of the waveform on pin OPA2 must be greater than a certain time. The minimum time is selected using the JMP1 pin.

Three different values can be programmed for the de-bounce time as shown in the table below.

JMP1	De-bounce time
Vss	1 to 2 msec
Floating	9 to 10 msec
Vdd	63 to 65 msec

Externally Programmable Detect Counter

The second logic block to assist in false trigger prevention is the Detect Pulse Counter. The de-bounced detect pulse clocks a counter. The count must reach a programmed number to generate an alarm condition. The counter will be reset back to zero if the time between any two valid detect pulses is longer than 20 seconds.

The 20 second time-out is reset with each valid detect pulse. For example if the max. count required is 2, the second pulse must occur within 20 seconds of the first pulse, or the counter will be reset back to 0.

With no incoming detection pulses, the counter is reset every 20 seconds. The device can select counts (ticks) of 1, 2, or 3. See the Product Options section for alternatives.

The count is externally selected by the voltage at the JMP2 pin.

JMP2	Count
Vss	1
Floating	2
Vdd	3

Post Alarm Dead Time.

When the Detect Counter reaches the programmed max. count, the ASIC opens the module output switch for 2.5 seconds to signal the alarm condition to the control panel. The LED output will also be pulsed ON for 2.5 seconds. At the end of this time the output switch is closed again and the LED switched off. Normally the circuit would then be able to respond to the next signal from the PIR element.

The switching of the output switch and LED are liable to cause some disturbance to the sensitive detection circuits, which may take some time to recover due to the long time constants inherent in the filter circuit.

To prevent chain reaction alarms, a 1,5sec dead time is provided to allow the op-amp and filter circuits to settle after the output switch and LED is switched off. During the 2.5 sec Alarm time and the 1.5 seconds dead time, new Alarm detects outputs are disabled at the window comparator.

Multi-Mode LED Indicator.

The SF389 provides direct drive to an LED indicator with an external resistor to set the current. The ALARM module LED would normally be off and pulsed on for 2.5 seconds whenever an alarm condition is detected. In addition, the ASIC has three different FLASH modes that are used to indicate:

a) the settling timeout after power on.
b) a module supply under-voltage or
c) the first to alarm latch has been set.

The sequences are shown below.

Mode a)	**Mode b)**	**Mode c)**
ON, 0.5 sec	ON, 0.5 sec	ON, 0.5 sec
OFF, 3.5 sec	OFF, 0.5 sec	OFF, 0.5 sec
ON, 0.5 sec	ON, 0.5 sec	ON, 0.5 sec
OFF, 3.5 sec	OFF, 2.5 sec	OFF, 1.5 sec
Repeats for 64 secs.	Repeats continuously	Repeats continuously

Latched Alarm Function.

The PIR389 can provide the user with a latched alarm, or First To Alarm function (FTA) The FTAC pin of the ASIC would normally switched from the panel to control the setting and resetting of the latched alarm state.

The FTA function is implemented in the following manner :-
When the control receives an alarm, the FTAC pin is pulsed from logic 0, (less than 0.5V) to logic I (greater than 2.5V). The low to high transition of FTAC latches the alarm state of the module in the chain that initiated the alarm. The flash sequence of the LED in that module then indicates the Latched alarm condition.

Although the output switch will close after 2.5 seconds, the latched indication will remain. The latching occurs on the low to high edge of the FTAC control line. The FTAC line goes to all the modules in a chain, however only the one in the alarm condition is latched. The latched alarm condition is cleared by a further low to high transition of the FTC control input, which must occur more than 4 seconds after the first latch pulse.

Alarm Output Driver

The output driver is configured as an electronic switch accessed via pins SW1 and SW2. The ON resistance of the output switch is typically less than 50Ω.
The output switch can be used to drive a small electromechanical relay reference to either Vdd or Vss. If a relay is used the output should be protected against the relay coil voltage fly-back by using a relay with an integral coil protection diode, or an external diode or Zener diode.

A typical coil resistance for a small 12V PCB reed relay is 1K. With 12V across the coil, the current in the driver and coil would be 12mA and the voltage drop across the output driver would be 600mV. If a free wheel diode is connected across the relay coil, separate protection may be required to prevent excessive current being forced into the ASIC via the relay output in the event of power supply reversal.

Power Up Time Out

The SF389 ignores inputs from the PIR element for the first 64 seconds after power up. The ASIC has an internal power on reset circuit to start the time out. If the power supply falls below around 4V, the ASIC is held in a reset condition. Provided there is sufficient supply voltage, the alarm output switch is held closed during this time-out. See Product Options for alternatives.

This time out is to allow the filter circuit capacitors to charge up, and the detection circuit to reach its operating condition. At the end of this time, which is indicated by the flashing sequence of the LED, the module can be walk tested to check the function.

Low Supply Indicator

The ASIC has a built in supply voltage level detection circuit. If the module supply voltage should fall below approx. 8V, the low supply LED flash sequence will start and the alarm output switch will open.

See Product Options for alternatives.
A hysteresis of approx. 0.2V is provided between the low supply condition being initiated on a falling supply, and the low supply condition being removed on a rising supply. This is to prevent confusing cycling of the LED indicator or opening or closing of the output switch due to ripple on the supply when it is close to the low voltage the trip point.

LED Control Function (LEDC)

The LEDC pin allows the indicator LED to be disabled from the control panel. The LEDC connection point of the module would be wired back to a logic output from the panel. All modules, for which this function is required in a system, would have their LEDC connection connected together.

If the LEDC pin of the ASIC is floating ,shorted to Vss, or driven to logic 0 at the panel , the LED functions are enabled. If the LEDC pin is driven to logic I, (more than + 2.5V above panel 0V) the LED functions are disabled.

LED Output Driver

The LED driver is open drain p channel transistor connected positive supply, Vdd. The driver can source up to 20mA for driving an LED through an external current limiting resistor. The nominal drive current would typically be 10mA, and the max voltage drop across the driver for this current would be 1.0V.

Product Options

The information presented in the previous sections defines the most flexible configuration of the device. The chip design allows for modifications to the following sections of the IC:

- Removal of ambient temperature compensation feature
- Alternative programmable count values in the range 1 to 7
- Output switch open during power up timeout condition.
- Output switch closed during under voltage condition.
- Reduced pin count or alternative packages.

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Contact the factory sales team to discuss these options.

7.0 APPLICATIONS INFORMATION

7.1 PARTS TABLE

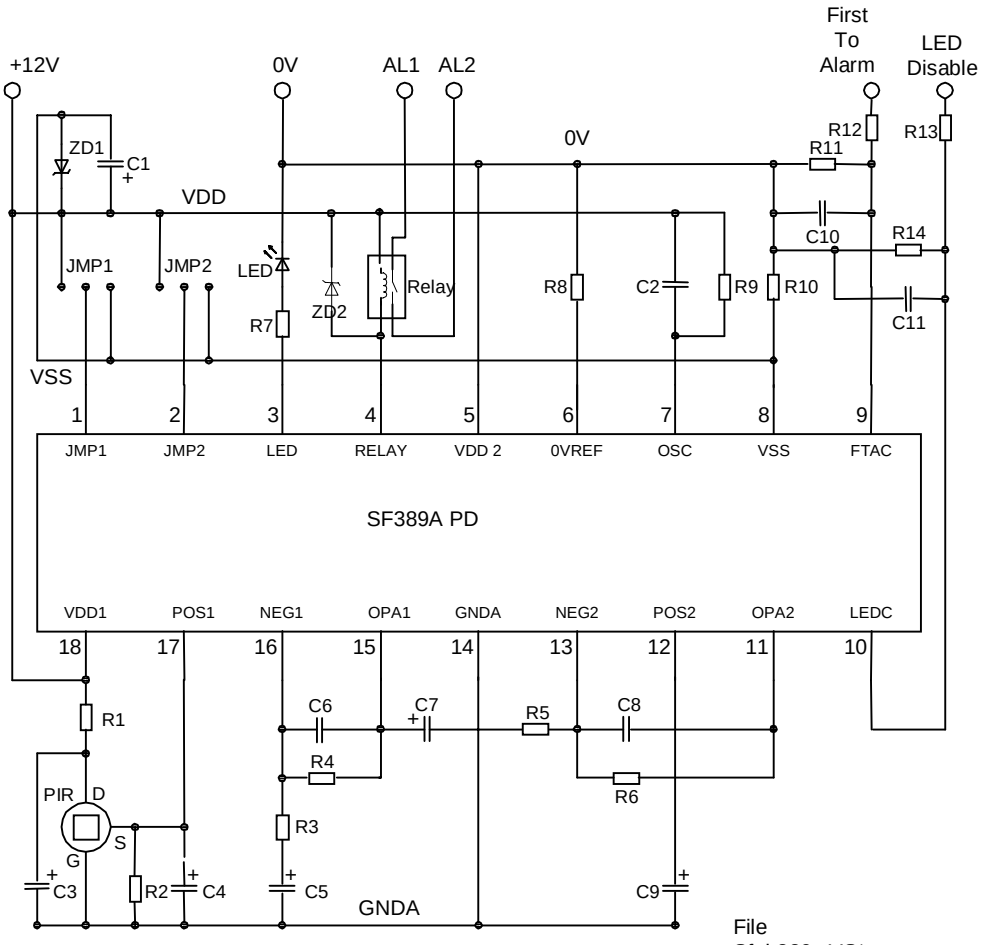
Note that these schematic diagrams and parts lists should be used for reference purposes only. Because of effect of the PCB layout, the component tolerances, and variations of components from different suppliers, no guarantees can be given regarding the performance of these circuit examples

PART	VALUE	COMMENT
R1	3K3	
R2	47K	
R3, R5	18K	
R4, R6	1MEG	
R7, R8	1K	1/4 W
R9	470K	1%
R10	390R	1W (note 2)
R11, R12, R13, R14	10K	
C1	47µF, 16V	
C2	1nF	NPO
C3, C5, C7	47µF, 10V	
C4	470pF	
C6	47nF	
C8	10nF	
C9	10µF, 10V	
C10, C11	100nF	
ZD1, ZD2	18V ZENER	1/2W, +/- 10% (notes 3 & 4)
RELAY	12V COIL	Coil resistance typ 1K

Note1: Unless stated otherwise, resistors are carbon film, 1/8 or 1/4W, *5%*
Note2: To withstand the current with reverse battery at 16V, IW rating required.
Note3: ZDI protects the ASIC from high voltage transients on the power line.
Note4: ZD2 protects the relay output of the ASIC from the coil flyback. A signal diode across the coil can perform this function, however a high current would flow in the diode and ASIC output in the event of battery reversal.

7.2 CIRCUIT DIAGRAM

18 Pin Version of PIR Alarm Module with First to Alarm control and LED control



JMP1 connection	De-bounce time	JMP2 connection	Count
Vss	1 – 2 ms	Vss	1
Floating	9 – 10 ms	Floating	2
Vdd	126 – 130 ms	Vdd	3

It is possible to dispense with the relay in some applications because the internal function connected to pins Relay and Vdd2 is a fully floating analogue switch.
Contact the factory for more details.

8.0 ORDERING INFORMATION

Order products using the following code:

SF389H PD for 18 pin PDIP package

Preliminary datasheets contain specifications based on prototype analysis and are current on publication date.

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